2. (Unamended) Security system according to claim 1, wherein at least said logic circuitry of the chips of said part of the secure devices is implemented in Field Programmable Gate Array FPGA technology, wherein the layout is programmed in the FPGA circuitry in at least one of a volatile and a non-volatile manner.

3. (Unamended) Security system according to claim 2, wherein the logic circuitry of each secure device chip is provided in a secure cell of the chip.

4. (Unamended) Security system according to claim 1, wherein the complete secure device ship is implemented in FPGA technology, wherein the layout is programmed in the chip in at least one of a volatile and a non-volatile manner.

5. (Unamended) Security system according to claim 2 wherein at least one of the logic circuitry and the entire chip is made as a volatile programmable FPGA, wherein the FPGA program is stored in a battery powered RAM.

E2 sub Ft

6. (Amended) A set of secure devices for a security system according to claim 1, wherein each of said secure devices comprises a chip with logic circuitry having a function in providing authorization to the holder of a secure device, wherein in at least a part of said secure devices, the chip of each secure device is provided with a unique chip layout, having the same functionality.

7. (Unamended) A set according to claim 6, wherein at least said logic circuitry of the chips of said part of the secure devices is implemented in FPGA technology, wherein the layout is programmed in the FPGA circuitry in at least one of a volatile and a non-volatile manner.

E3 sub Ft

8. (Amended) Method for manufacturing a secure device for a security system according to claim 1, wherein secure devices with a chip are used, said chips having logic circuitry having a function in providing authorization to the security system, wherein in at least a part of said secure devices, the chip of a secure device is provided with a unique chip layout, having the same functionality.

9. (Unamended) Method according to claim 8, wherein chips with logic circuitry in FPGA technology are use, said method comprising programming a unique information in the logic circuitry utilizing a synthesis tool and a layout tool, wherein for each secure device of said part of secure devices, a variation factor is introduced in at least one of the synthesis tool and the layout tool, thereby providing a unique circuit layout.

10. (Unamended) Method according to claim 9, wherein the synthesis tool is provided with input information compiled from a high level language code, wherein a variation factor is introduced in at least one of the compilation step of the high level language code, the synthesis tool and the layout tool.